#### Make or Break

The Big Impact of Small Changes on Performance in Java Programs





# Yes you can





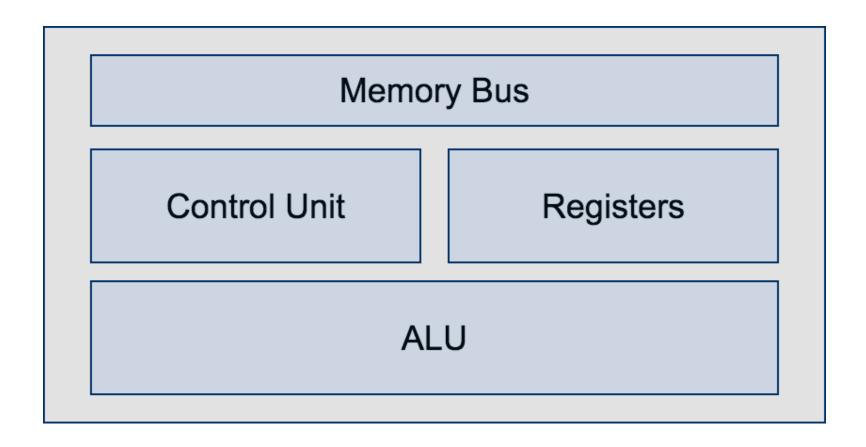
# Components



# Mechanical Sympathy



#### What's in a CPU?







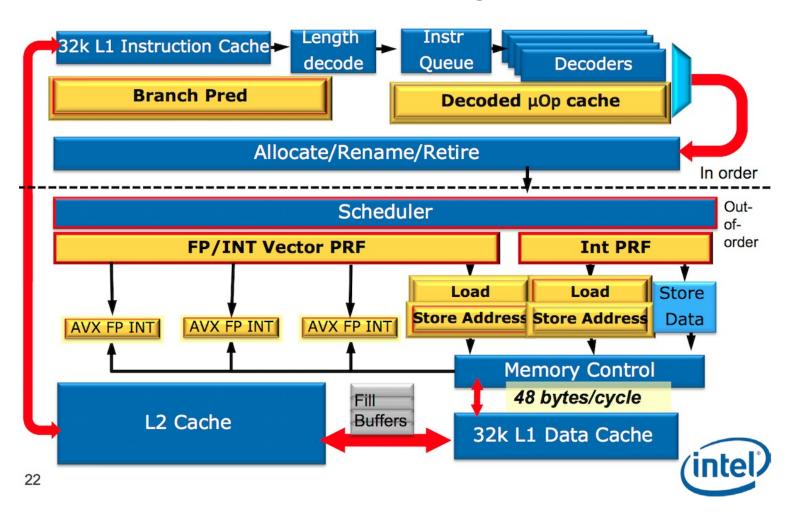
# Pipelining



# Experiments

#### Hardware: x86

i7-2635QM (Sandy-Bridge quad-core)

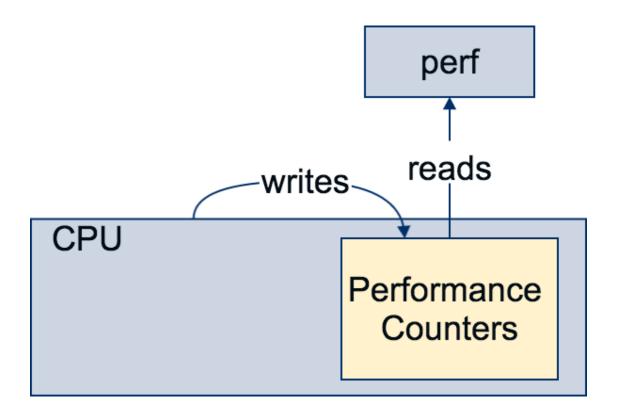


#### Software: JMH

- The microbenchmarking framework on the JVM
- In a nutshell: Add @Benchmark; JMH takes care of the rest\*
- perf support

Intro to JMH: Tomorrow, 13:00 in room "Quantum 2"

#### man perf



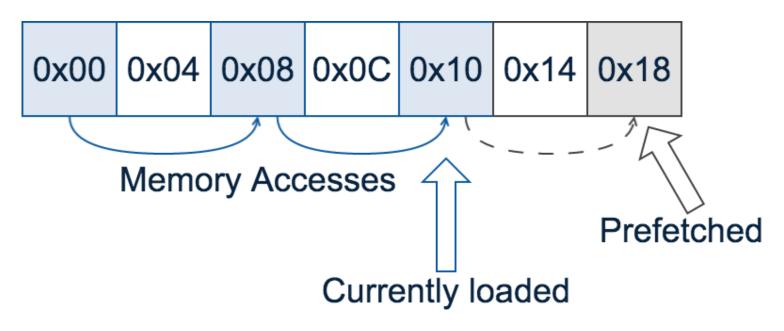
# Experiments

- To Prefetch or not to Prefetch?
- False Sharing
- Puzzling Branch Prediction

#### To Prefetch or not to Prefetch?

# Prefetching Unit

CPU speculatively loads data based on memory access patterns



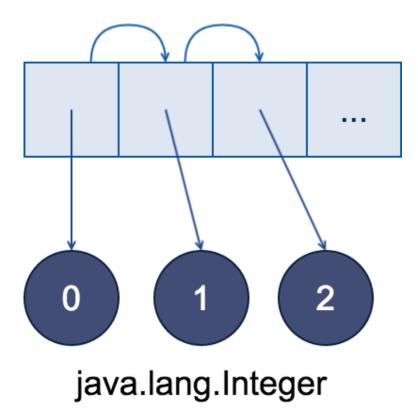
# Contenders: int[]

Contiguous array: Linear memory access pattern for traversal:



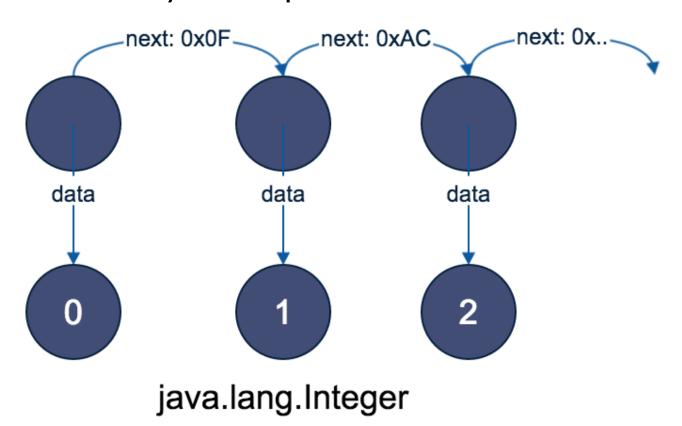
### Contenders: ArrayList

Linear memory access pattern for array traversal; pointer chasing for elements:



#### Contenders: LinkedList

Nonlinear memory access pattern for traversal and elements:



# Experiment Setup

• Task: Calculate the sum of all elements

#### Benchmark: Setup LinkedList

```
@State(Scope.Benchmark)
public class PointerChasingBenchmark {
    @Param({"1024", "2048", "4096", "8192", "16384", "32768"})
    public int problemSize;

    private final List<Integer> linkedList = new LinkedList<>();

    @Setup
    public void setUp() {
        for (int idx = 0; idx < problemSize; idx++) {
            linkedList.add(idx);
        }
    }
} // ...
}</pre>
```

Note: the other setup methods are identical except for their type

#### Benchmark: LinkedList

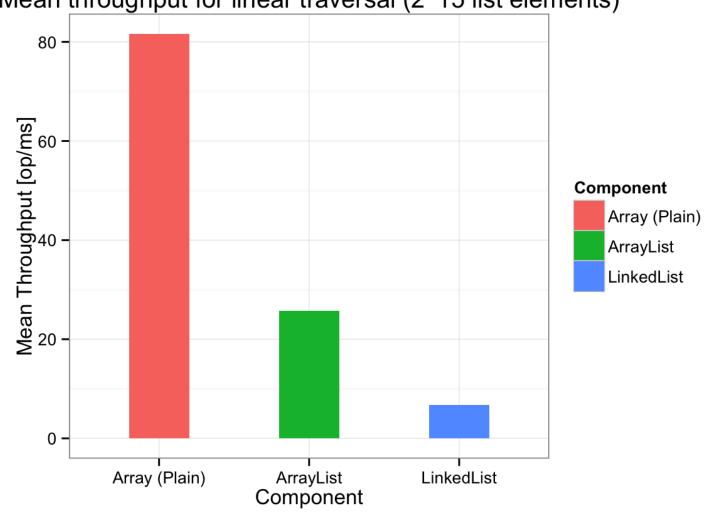
```
@State(Scope.Benchmark)
public class PointerChasingBenchmark {
    // .. Setup ..

    @Benchmark
    public long sumLinkedList() {
        long sum = 0;
        for (int val : linkedList) {
            sum += val;
        }
        return sum;
    }
}
```

Note: the other benchmark methods are identical except for their type

#### Results





# Why the difference?

Read CPU performance monitoring data with JMH's perf profiler

Metric	int[]	ArrayList	LinkedList
L1-dcache-loads	61 * 10 <sup>9</sup>	58 * 10 <sup>9</sup>	21 * 10 <sup>9</sup>
L1-dcache-load-misses	6%	10%	22%
(relative to L1 cache hits)			

#### Conclusion

Pointer indirection renders prefetching ineffective

# Take Aways and Suggestions

- Memory access patterns matter: Prefer linear access
- Watch Oracle's work on Value Objects (JEP 169)

# False Sharing

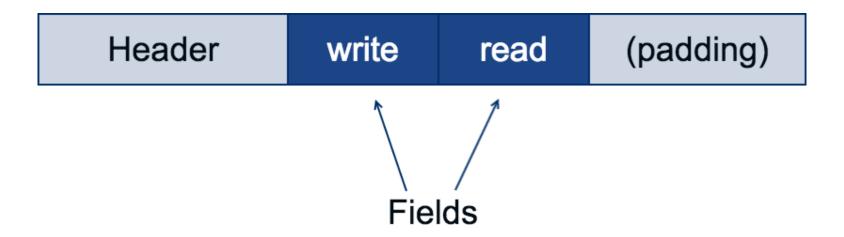
### Experiment Setup

 Task: Three readers and a writer access two unrelated fields of a shared object

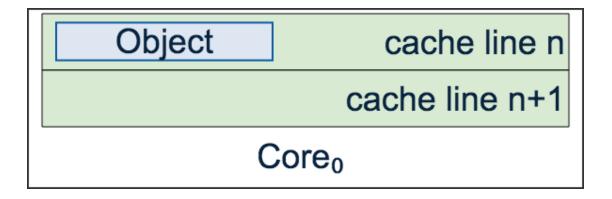
#### Benchmark

```
@Threads(4)
public class FalseSharingMicroBenchmark {
  @State(Scope.Benchmark)
 public static class FalselySharedState {
   public long write;
   public long read;
  @Group("false sharing")
  @GroupThreads(1)
  @Benchmark
 public void produce(FalselySharedState s) {
   s.write++;
  @Group("false sharing")
  @GroupThreads(3)
  @Benchmark
 public long consume(FalselySharedState s) {
   return s.read;
```

### A Java Object in Memory



#### The Processor's View



# False Sharing

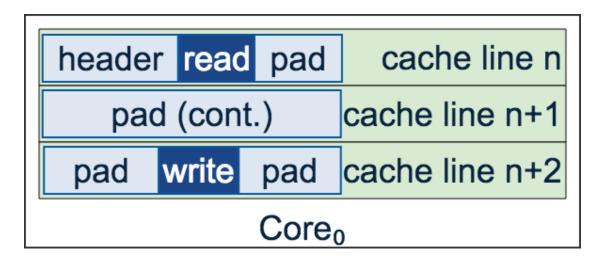


# False Sharing



#### Countermeasures

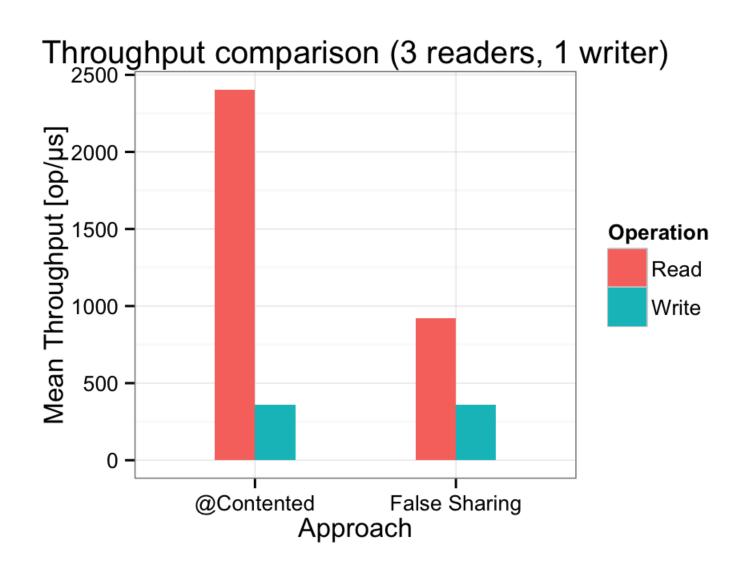
Field padding, e.g. with @sun.misc.Contended



#### Benchmark

```
@Fork(value = 5, jvmArgs = "-XX:-RestrictContended")
@Threads(4)
public class ContendedAccessMicroBenchmark {
  @State(Scope.Benchmark)
 public static class ContendedState {
    @Contended
   public long write;
   public long read;
  @Group("contended")
  @GroupThreads(1)
  @Benchmark
 public void produce(ContendedState s) {
   s.write++;
  @Group("contended")
  @GroupThreads(3)
  @Benchmark
 public long consume(ContendedState s) {
   return s.read;
```

## Results



## Why the difference?

Read CPU performance monitoring data with JMH's perf profiler

Metric	@Contended	False Sharing
L1-dcache-loads	231 * 10 <sup>9</sup>	96 * 10 9
L1-dcache-load-misses (relative to L1 cache hits)	0.01%	1.7 %

#### Conclusion

Increased bus traffic due to shared cache lines reduces throughput

## Take Aways and Suggestions

- Sometimes, object layout matters in multi-threaded code
- Use libraries like Nitsan Wakart's JCTools which implement countermeasures

## Puzzling Branch Prediction

Credits: Example based on a Stackoverflow discussion

#### **Branch Prediction**

Keep instruction pipeline full by guessing what will be done next

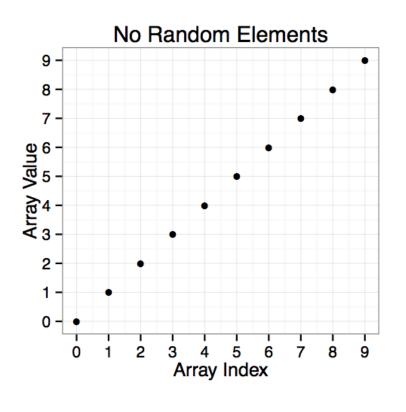
- Static branch prediction
- Dynamic branch prediction: Based on history
- Loop detector
- Meta-predictor

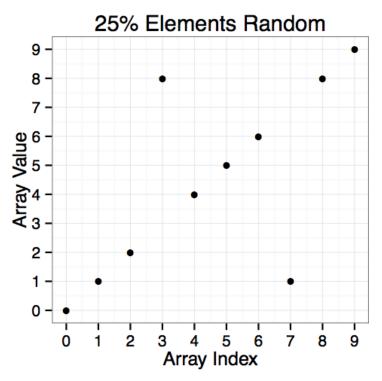
# Contenders: int[] sorted / unsorted

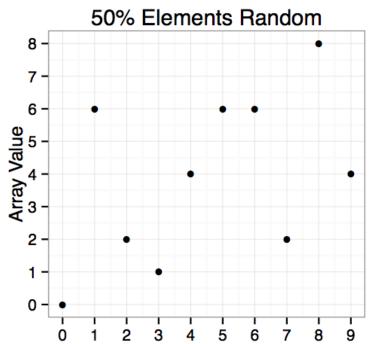
- Array size: 2<sup>16</sup> elements each
- Array values: [0, 255] randomly distributed

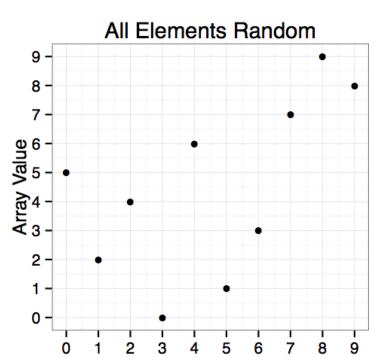
## Experiment Setup

• Task: Calculate the sum of all elements >= 128





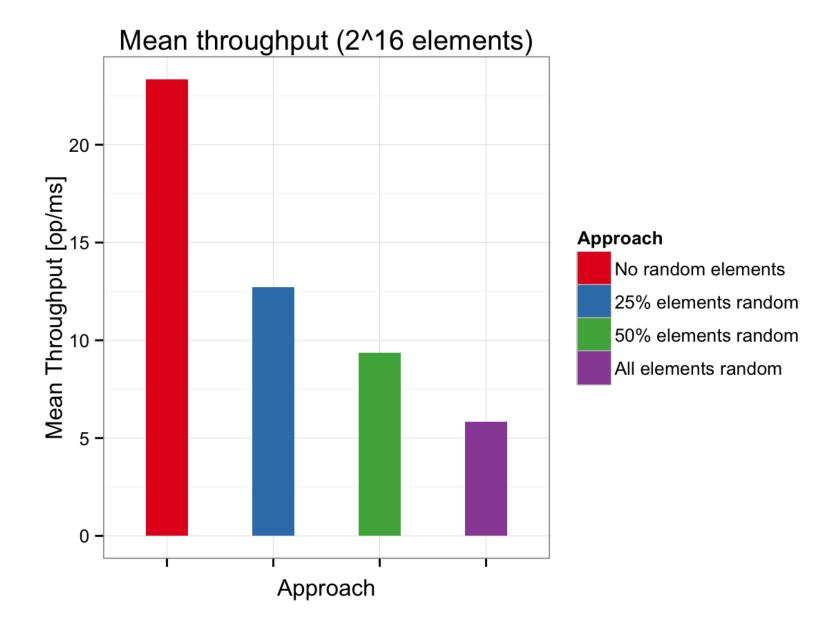




#### Benchmark

```
@Benchmark
public long benchmarkSum() {
  long sum = 0;
  for (int idx = 0; idx < array.length; idx++) {
    if (array[idx] >= 128) {
       sum += array[idx];
    }
  }
  return sum;
}
```

## Results



## Why the difference?

Read CPU performance monitoring data with JMH's perf profiler

Metric			50% random	100% random
branch-misses (relative to all branches)	0.02%	3.7 %	7.6%	16.8 %

#### Conclusion

Randomly taken paths render the branch predictor useless and stall the pipeline

## Take Aways and Suggestions

- Avoid branches in critical loops or...
- Make them predictable by following a common branching pattern

## Summary



## Understand Hardware Behavior

### Measure

#### Resources

Slides: http://bit.ly/java-cpu-talk-slides

Code: http://bit.ly/java-cpu-talk-code

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## Backup

## **CPU**

- Process model: i7-2635QM
- Micro architecture: Sandy Bridge

### CPU

```
cat /proc/cpuinfo #processor 0-7 -> HT enabled
                : 0
processor
vendor id
              : GenuineIntel
cpu family
                : 6
model
                : 42
model name
              : Intel(R) Core(TM) i7-2635QM CPU @ 2.00GHz
stepping
               : 7
microcode
               : 0x1a
cpu MHz
               : 800.312
cache size
              : 6144 KB
physical id
              : 0
siblings
                : 8
core id
                : 0
cpu cores
              : 4
apicid
               : 0
initial apicid
                : 0
fpu
                        : yes
fpu exception
                : yes
cpuid level
                : 13
wp
                        : yes
[...]
```

## **CPU**

#### OS

#### uname:

Linux 3.15.8-1-ARCH #1 SMP PREEMPT x86\_64 GNU/Linux